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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,123	12/13/2001	Sifen Luo	US 010624	2515

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Corporate Patent Counsel
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EXAMINER
NGUYEN, LINH V

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,123	LUO ET AL.	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☒ Claim(s) *23-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1-4, 7-8, 11- 14, and 18 – 22, are rejected under 35 U.S.C. 102(e) as being anticipated by Dening U.S. patent No. 6,333,677.

Regarding to claim 1, Fig. 7 disclose an RF power amplifier circuit comprising: sensing a collector current in an input stage transistor (112); feeding a current equal or proportional to said input stage transistor collector current (collector current 112) to an output stage bias circuit (118) to boost the bias of an output stage (106 collector output); wherein the input stage transistor is operated in a class AB mode (Col. 8 line 9), and said output stage is fed through a matching network (224).

Regarding to claim 2, wherein the input stage transistor collector current is sensed and fed to the output stage bias circuit via a current mirror (112, 114, Col. 5 lines 55 – 65).

Regarding to claim 3, wherein one transistor comprising said current mirror is connected in series with a transistor that itself forms a second current mirror with the input stage transistor (110, 112, 114).

Regarding to claim 4, wherein the amplifier circuit comprises plural bipolar junction transistors (Fig. 7)).

Regarding to claim 7, Fig. 7 Dening discloses transistor circuit, comprising: an input stage (RF In); an output stage with a biasing circuit (106 collector current); and a current mirror (112), which senses an input signal current and feeds a current proportional to said input signal current to an output stage biasing circuit (118).

Regarding to claim 8, wherein said current mirror includes at least one BJT (110).

Regarding to claim 11, Fig. 7 Dening discloses method boosting the output stage bias of an amplifier circuit, comprising: sensing an input signal (112); and boosting an output stage bias (114) with a current equal or proportional to the input signal

Regarding to claim 12 where the input signal is an RF signal (102) .

Regarding to claim 13, where the input signal is sensed by a current mirror (112).

Regarding to claim 14, wherein a collector current of an input stage BJT is mirrored by the current mirror and fed into an output stage biasing circuit (110,112, 114).

Regarding to claim 18. Fig. 7 Dening discloses a sub-circuit (110), to be used in an amplification circuit, comprising: an input sensor (112), arranged to sense an input signal to the amplification circuit, and an output stage booster (112), arranged to boost a bias of an output stage of the amplification circuit in proportion to said input signal.

Regarding to claim 19, where the input signal is an RF signal (102).

Regarding to claim 20, where the input sensor is a current mirror (112).

Regarding to claim 21. (New) Fig. 7 Dening discloses bias boosting sub-circuit (110) for a multi-stage power amplifier circuit, said multistage power amplifier comprising at least an input stage and an output stage, said sub-circuit comprising: two matched BJTs in a first current mirror (106,112, 114), wherein the first current mirror (114) senses a collector current of an amplifying transistor (112) in the input stage, and feeds an equal or proportional current to a bias circuit (110) of the output stage (106 collector).

Regarding to claim 22, wherein one of the transistors of the first current mirror is connected in series with a third transistor (106, 112, 114)), said third transistor itself forming a second current mirror with the input stage amplifying transistor.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5, 6, 9, 10, and 15 – 17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dening

Fig. 7 Dening as applied to claims, 7, and 13 above disclose every aspect of applicant's claimed invention except for amplifier circuit having field effect transistors

(FET). However using FET in RF amplifier circuit is a well known art and conventional, one of ordinary skill in the art, furthermore, would have expected Application's invention to perform equally well with BJT amplifier circuit of Dening because applicant's specification and figures of this application do not teach or show any structures related to claimed invention, and provides an advantage is used for particular purpose, or solves a stated problem. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was mad to modify BJT amplifier circuit to FET amplifier circuit.

Allowable Subject Matter

4. Claims 23 – 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned

are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

April 1, 2003

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800